PDR RID Report

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Document CSMS Requirements Spec (304-CD-003-001)

Section 6.3.5.1 **Page** 6-33,34 **Figure Table** NA

RID ID PDR 206
Review CSMS
Originator Ref
Priority 2

Category Name Design-CSS **Actionee** HAIS

Sub Category

Subject Need to specify the relationship between time services

Description of Problem or Suggestion:

This section specifies a series of time oriented service based upon UTC time and synchronized to various time providers "such as radios, satellites, or telephone lines. It is unclear how this relates to specification elsewhere (ex. 4.2.2.3.5) that NASA 36 bit serial time code is the reference time for all processors.

It would be advisable to add to the time service requirements that all time adjustments be made in such a manner that local system is always monotonically increasing.

Originator's Recommendation

Review and revise if deemed appropriate

GSFC Response by: **GSFC Response Date**

HAIS Response by: Forman **HAIS Schedule** 2/28/95

HAIS R. E. Baker **HAIS Response Date** 3/6/95

CSS is presenting a design that provides an NTP server feed at every DAAC, the EOC, and the isolation cell. The NTP server will function as the System Time Provider source to the DCE Distributed Time Service (DTS) Servers within each DCE cell. Alternatives are now being evaluated regarding the source for these Time Servers. The alternatives include NASA-36 or GPS. CSMS feels that this approach will allow V0 and DTS interoperability and a NASA-36 or GPS source will provide a single time for the entire network.

The Distributed Time Service (DTS) synchronizes the system clock on each host by directly adjusting the time kept by the operating system. Under ordinary circumstances, this is done gradually so that there are no sudden jumps in the time. It is also done in such a way that the time never goes backward. If a system clock is too far ahead, it is slowed down until the time is correct by modifying the tick increment. In other words, if a clock is normally incremented 10 milliseconds at each clock interrupt, and the clock is ahead, then the clock register will instead be incremented 9 milliseconds at each clock time until it reaches the correct time.

The requirements documents will be updated as required by CDR.

Status **Closed** **Date Closed** **3/28/95** **Sponsor** **Broder**

****** **Attachment if any** ******